Abstract of the Disclosure:

A transistor array has vertical FET transistors each connected to a storage capacitor of a memory cell array. Gate electrode strips, which form word lines, of the transistors are located on both sides of active webs running parallel to one another and are connected to a superimposed metal plane by word line or CS contacts. To insulate these word line contacts from the other elements of the transistor array and of the cell array, the word line contacts are located in deep trenches that are introduced into the webs.

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